

EAST - [10799060.wsp:1]

File View Edit Tools Window Help

Drafts Pending Active

L1: (60563) non-volatile near memory non near volatile near memory and (shallow near trench near..

L3: (1) ("6046935").PN.

L4: (1) ("5070032").PN.

L5: (1) ("5315541").PN.

L6: (1) ("5343063").PN.

L7: (1) ("5661053").PN.

L8: (1) ("6281075").PN.

L9: (1) ("5313421").PN.

L10: (1) ("6222762").PN.

L11: (408) 2 and floating adj gate adj structure

L12: (60562) non-volatile near memory non near volatile near memory and (shallow near trench near..

L12: (0) 2 and floating adj gate adj structure and recess and protrusion

L13: (37) 2 and floating adj gate adj structure and recess

L14: (104) 1 and poly2

L15: (17) 1 and poly2 and (shallow near trench near isolation STI)

L16: (1) ("5089867").PN.

L17: (1) ("6111788").PN.

L18: (1) ("6287915").PN.

L19: (1) ("6204120").PN.

Failed

1 and poly near 2

Saved

Favorites

Tagged (0)

UDC

Queue

Trash

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DBs US-PGPU8:USPAT:USOCR Plurals

Default operator: OR Highlight all hit terms initially

1 and poly2

BRS form IS&R form Image Text HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050167731 A1	20050804	35	Double-cell memory device	257/315	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20050141298 A1	20050630	43	Combination nonvolatile memory using unified technology with byte, page and block write and simultaneous read and write operations	365/200	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20050026389 A1	20050203	11	Method for the fabrication of isolation structures	438/424	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20040214387 A1	20041028	20	Methods for fabricating three dimensional integrated circuits	438/200	438/241
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20040209472 A1	20041021	17	Method for manufacturing non-volatile memory cells on a semiconductive substrate	438/689	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20040203250 A1	20041014	9	Method for manufacturing non-volatile memory cells on a semiconductor substrate	438/727	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20040179392 A1	20040916	9	Non-volatile memory cell comprising dielectric layers having a low dielectric constant and corresponding manufacturing process	365/154	257/E21.682; 257/E27.103
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20040152260 A1	20040805	9	Non-volatile memory cell with non-uniform surface floating gate and control gate	438/257	257/E21.209; 257/E21.682; 257/E27.103;
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20040121589 A1	20040624	6	Process for contact opening definition for active element electrical connections	438/637	257/E21.576; 257/E21.577
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20040041200 A1	20040304	19	High density flash memory architecture with columnar substrate coding	257/316	257/E21.422
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20040027856 A1	20040212	45	Combination nonvolatile memory using unified technology with byte, page and block write and simultaneous read and write operations	365/185.11	257/E21.69; 257/E27.103; 365/185.33

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